Notice of Allowability	Application No.	Applicant(s)	
	10/807,527	SHIU ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/06/06*.

2. ☒ The allowed claim(s) is/are *1-6 and 8-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-6, and 8-20 are allowed.

2. The following is an examiner's statement of reasons for allowance:

The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

A method of packaging an integrated circuit die, comprising the steps of: providing a foil sheet; forming a single layer of solder on a first side of the foil sheet; attaching a first side of an integrated circuit die to the single solder layer on the foil sheet; electrically connecting the bonding pads of the die to the single solder layer on the foil sheet with a plurality of wires; and separating the foil sheet from the die and the plurality of wires, thereby forming a packaged integrated circuit, as recited in claim 1. Claims 2-6, and 8-14 are dependent upon independent claim 1.

A method of forming a plurality of integrated circuit packages, comprising the steps of: providing a sheet of metal foil; forming a layer of high temperature solder on a first side of the foil sheet via a screen printing process; attaching a first sides of a plurality of integrated circuit dies to the single solder layer on the foil sheet; electrically connecting the bonding pads of the dies to the single solder layer on the foil sheet with a plurality of wires via a wirebonding process; and separating the foil sheet and the solder layer from the integrated circuit dies, second ends of the plurality of wires, and the mold compound via a second reflow process, wherein only a portion of the solder layer is removed from the dies and the second ends of the plurality of wires, as recited in claim 15. Claims 16-17 are dependent upon independent claim 15.

A method of forming a multi-chip module, comprising the steps of: providing a sheet of metal foil; forming a single layer of high temperature solder on a first side of the foil sheet via a screen printing process; attaching a first sides of at least two integrated circuit dies to the single solder layer on the foil sheet; electrically connecting a first portion of the bonding pads of each of the at least two dies to the single solder layer on the foil sheet with a plurality of first wires via a first wirebonding process; and separating the foil sheet and the solder layer from at least two integrated circuit dies, second ends of the plurality of first wires, and the mold compound via a second reflow process, wherein only a portion of the solder layer is removed from at least two dies and the second ends of the plurality of wires, as recited in claim 18. Claims 19-20 are dependent upon independent claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
20 Feb. 2007